REMARKS/ARGUMENTS

Claims 1-48 are pending in the present application. Reconsideration of the claims is respectfully requested.

I. 35 U.S.C. § 102, Asserted Anticipation, Claims 1-48

The Examiner rejected claims 1-48 under 35 U.S.C. § 102(b) as anticipated by *Jeddeloh*, System and Method for Remapping Defective Memory Locations, U.S. Patent No. 6,052,798 (July 1, 1988) (hereinafter "*Jeddeloh*"). This rejection is respectfully traversed.

With regards to claims 1, 17, and 33, the Examiner states:

> With respect to claims 1, 17, and 33, Jeddeloh discloses a computer program/method in a data processing system including a storage drive for verifying a condition of said storage drive's media, comprising:
> A) receiving within said storage drive a command to verify said condition of said storage drive's media ***(step 64, a memory access request is received from a memory requester, such as the system processor);***
> B) in response to a receipt of said command, attempting, by said storage drive, to read each one of a plurality of logical block addresses included in said storage drive ***(the memory access request to include an indication of whether a read or a write is being requested together with an address of the requested memory portion of the memory block);*** and
> C) verifying said condition of said media by determining, by said storage drive, ones of said plurality of logical block addresses that are not in a readable condition ***(step 66 determines whether the requested memory portion of the memory block is defective)*** **[See *steps 64 and 66, Fig. 3; Col. 5, Lines 51- 61).***

Office Action dated December 14, 2005, pages 2-3.

A prior art reference anticipates the claimed invention under 35 U.S.C. § 102 only if every element of a claimed invention is identically shown in that single reference, arranged as they are in the claims. *In re Bond*, 910 F.2d 831, 832, 15 U.S.P.Q.2d 1566, 1567 (Fed. Cir. 1990). All limitations of the claimed invention must be considered when determining patentability. *In re Lowry*, 32 F.3d 1579, 1582, 32 U.S.P.Q.2d 1031, 1034 (Fed. Cir. 1994). Anticipation focuses on whether a claim reads on the product or process a prior art reference discloses, not on what the reference broadly teaches. *Kalman v. Kimberly-Clark Corp.*, 713 F.2d 760, 218 U.S.P.Q. 781 (Fed. Cir. 1983). In this case each and every feature of the presently claimed invention is not identically shown in the cited reference, arranged

as they are in the claims.

Claim 1 is as follows:

> 1. (Original): A method in a storage drive for verifying a condition of said storage drive's media, said method comprising the steps of:
> receiving within said storage drive a command to verify said condition of said storage drive's media;
> in response to a receipt of said command, attempting, by said storage drive, to read each one of a plurality of logical block addresses included in said storage drive; and
> verifying said condition of said media by determining, by said storage drive, ones of said plurality of logical block addresses that are not in a readable condition.

Regarding claim 1, *Jeddeloh* fails to teach the claimed step of receiving a command to *verify* the condition of the storage drive's media. The Examiner asserts otherwise, citing the following portions of *Jeddeloh* (emphasis added):

> In step 64, a memory access request is received from a memory requestor, such as the system processor 24. The memory access request can be a request to *write* data to or *read* data from a requested memory portion of the volatile memory block 14.

Jeddeloh, Column 5, Lines 51-56.

This portion of *Jeddeloh* teaches receiving a *write* data request or a *read* data request from a portion of a volatile memory block. However, neither this portion of *Jeddeloh* nor any other portion of *Jeddeloh* teaches receiving a command to *verify* a portion of a volatile memory block. A verify command is different than a write data request or a read data request. Accordingly, *Jeddeloh* does not anticipate claim 1, which requires a request to verify.

Furthermore, no indication exists in the cited sections of *Jeddeloh* for receiving a command to verify the condition of a ***storage drive's media***. Instead, *Jeddeloh* teaches a memory module comprising a *volatile* memory block, a nonvolatile memory block having an error map, and a remapping table in the volatile memory block (*Jeddeloh*, claim 1). Fig. 1 of *Jeddeloh* shows memory module **12** as a distinct component from hard drive **32**, where "hard drive **32** ... is a ***nonvolatile*** memory device" (emphasis added). *Jeddeloh* Column 3, Lines 28-32. Thus, *Jeddeloh* is concerned with write and read requests to a *volatile* memory module, in contrast to the present invention which deals with verifying

the condition of a *storage driver's media*. Accordingly, both the command being performed and the component the command is performed on in *Jeddeloh* are different than the invention of claim 1. Additionally, *Jeddeloh* does not elsewhere teach receiving a command to verify the condition of a storage drive's media.

As shown above, *Jeddeloh* does not teach at least two features of claim 1. Because *Jeddeloh* does not teach all the features of claim 1, *Jeddeloh* does not anticipate claim 1.

Because claims 2-16 depend from claim 1, the same distinctions between *Jeddeloh* and the invention of claim 1 can be made for these claims. Additionally, claims 2-16 claim other additional combinations of features not suggested by *Jeddeloh*. The Examiner does not assert that the other references teach or suggest these claimed features, and the other references do not actually teach or suggest these claimed features. Consequently, Applicants respectfully urge that the rejection of claims 1-16 has been overcome.

Claims 17-32 claim data processing systems implementing the methods of claims 1-16. Therefore, the same distinctions between *Jeddeloh* and the inventions of claims 1-16 can be made for claims 17-32. Consequently, Applicants respectfully urge that the rejection of claims 17-32 has been overcome.

Claims 33-48 claim computer program products implementing the methods of claims 1-16. Therefore, the same distinctions between *Jeddeloh* and the inventions of claims 1-16 can be made for claims 33-48. Consequently, Applicants respectfully urge that the rejection of claims 33-48 has been overcome.

II. 35 U.S.C. § 103, Asserted Obviousness, Claims 6-9, 22-25, and 38-41

The Examiner rejected claims 6-9, 22-25, and 38-41 under 35 U.S.C. § 103(a) as obvious over *Jeddeloh* in view of *Reeve* et al., Small Computer Systems Interface – Data Link Processor, U.S. Patent No. 4,864,532, (Sep. 21, 1987) (hereinafter "*Reeve*"). This rejection is respectfully traversed.

If the Patent Office does not produce a *prima facie* case of unpatentability, then without more the applicant is entitled to grant of a patent. *In re Oetiker*, 977 F.2d 1443, 1445, 24 U.S.P.Q.2d 1443, 1444 (Fed. Cir. 1992); *In re Grabiak*, 769 F.2d 729, 733, 226 U.S.P.Q. 870, 873 (Fed. Cir. 1985). A prima facie case of obviousness is established when the teachings of the

prior art itself suggest the claimed subject matter to a person of ordinary skill in the art. *In re Bell*, 991 F.2d 781, 783, 26 U.S.P.Q.2d 1529, 1531 (Fed. Cir. 1993). All limitations of the claimed invention must be considered when determining patentability. *In re Lowry*, 32 F.3d 1579, 1582, 32 U.S.P.Q.2d 1031, 1034 (Fed. Cir. 1994). A proper *prima facie* case of obviousness cannot be established by combining the teachings of the prior art absent some teaching, incentive, or suggestion supporting the combination. *In re Napier*, 55 F.3d 610, 613, 34 U.S.P.Q.2d 1782, 1784 (Fed. Cir. 1995); *In re Bond*, 910 F.2d 831, 834, 15 U.S.P.Q.2d 1566, 1568 (Fed. Cir. 1990).

II.A. The Examiner Has Failed to State a Prima Facie Obviousness Rejection Against Claims 6 and 9

II.A.1 All of the Features of Claim 6 Are Not Present in the Cited References

The features that the Examiner states as being present in the references are not found or suggested by the references. Claim 6 is as follows:

> 6. The method according to claim 1, further comprising the steps of:
> receiving within said storage drive said command to verify said condition of said storage drive's media from a host computer system;
> in response to a receipt of command by said storage drive, said storage drive disconnecting itself from host; and
> verifying, by said storage drive, said condition of said media while said storage drive is disconnected from said host.

First, neither *Jeddeloh* nor *Reeve* teach or suggest, individually or in combination, the claimed step of receiving within the storage drive the command to *verify* the condition of the storage drive's media from a host computer system. Similarly, the Examiner does not assert that *Jeddeloh* or *Reeve* teach or suggest receiving a command to verify. For this reason alone, the proposed combination does not teach all of the features of claim 6, and the Examiner has accordingly failed to state a prima facie obviousness rejection against claim 6.

Second, neither *Jeddeloh* nor *Reeve* teach or suggest, individually or in combination, the claimed step of verifying, by the storage drive, the condition of the media while the storage drive is disconnected from the host. The Examiner admits that *Jeddeloh* fails to teach verifying the condition of the media while the storage drive is disconnected from the host. However, the

Examiner asserts that *Reeve* teaches verifying the condition of the media, by the storage drive, while the storage drive is disconnected from the host in col. 12, lines 4-31. Office Action dated December 14, 2005, page 6. However, the Examiner's interpretation of this cited reference is incorrect.

With regard to claim 6, the Examiner states:

> Jeddeloh discloses
> A) the memory device being nonvolatile memory such as EEPROM or flash memory [Col. 3, Lines 6-10; Col. 3, Lines 41-45] the memory being coupled through memory and expansion bus 26, Fig. 2; but fails to specifically teach coupling and decoupling itself from the host.
> B) However, Reeve discloses sequence of operations operated in the sequential handling of data transfer operations where disk drive reconnects and disconnects itself to/from to data link processor in the process of transferring data complete I/O cycled operations [Col. 12, Lines 4-31]. Therefore, it would have been obvious to one of ordinary skill in the art, that storage medium couples and decouples itself from the host, as taught by Reeve, in order to continue an operation which was previously started by the data link processor.

Office Action dated December 14, 2005, page 6.

The cited portions of *Reeve* are as follows:

> The disk drive 51 may need time to cross a "cylinder boundary" or else to perform some other time-consuming task. Therefore, the disk drive 51 disconnects from the SCSI-DLP 20, and the DLP 20 itself unit queues will save the present data pointers (the S register address and the P register address) in the appropriate scratchpad queue portion of the segmented buffer memory 24 which is addressed by the SPAD 30 (scratch pad address register).
>
> After the disconnection process takes place, the SCSI-DLP 20 is now available to receive more I/O descriptors from the host computer 10 or else to issue a command to another disk drive--all the time while the DLP is waiting for the disk drive 51 or the disk drive 52 to reconnect itself to the DLP 20.
>
> As another example, if the disk drive 52 has found its requested sector of data and then reconnects to the DLP (as disk drive 51 did earlier) and the disk drive 52 then begins data transfer just like disk drive 51 did, it should, however be understood that the disk drive 52 will be transferring its data into the segment known as page two of the segmented buffer memory 24 which is dedicated to the disk drive 52.
>
> Thus, it can be seen that there are two data transfers which are in process

simultaneously and at the same time.

It can be noted here that the SCSI-DLP 20 did not have to flush out the contents of the (page one) section of its remaining data before allowing the transfer of data into page 2 for the disk drive 52. This was done because the data was simply put into another page.

Reeve, Column 12, Lines 1-31.

As can be seen, this portion of *Reeve* teaches that during a data transfer, when the disk drive needs time to perform a task such as crossing a cylinder boundary, it disconnects, performs the task, and then reconnects to resume the data transfer. During the time the disk drive is disconnected, the data is transferred into a buffer memory, and when the disk drive reconnects, the data transfer resumes from the buffer memory. The reason for performing these actions is to increase the data transfer rate between the host computer and the disk drives. See also *Reeve*, Abstract.

However, neither the cited portion of *Reeve*, nor any other portion of *Reeve* teaches or suggests *verifying the condition of the media* while the storage drive is disconnected from the host, as recited in claim 6. Therefore, *Reeve* does not teach or suggest the features of claim 6, as asserted by the Examiner. In addition, *Reeve* does not elsewhere teach or suggest the claimed features, as asserted by the Examiner.

II.A.2 <u>All of the Features of Claim 9 Are Not Present in the Cited References</u>

The features that the Examiner states as being present in the references are not found or suggested by the references. Claim 9 is as follows:

> 9. The method according to claim 1, further comprising the steps of:
> coupling said storage drive to a host utilizing a SCSI bus;
> receiving within said storage drive said command to verify said condition of said storage drive's media utilizing said SCSI bus; and
> said command being a SCSI command.

Neither *Jeddeloh* nor *Reeve* teach or suggest, individually or in combination, the claimed step of receiving within the storage drive the command to *verify* the condition of the storage drive's media utilizing the SCSI bus. The Examiner admits that *Jeddeloh* fails to teach coupling said storage drive to a host utilizing a SCSI bus. The Examiner next asserts that *Reeve* teaches "sequence of operations operated in the sequential handling sequential handling of data transfer

operations Small computer systems interface (SCSI) bus" in the abstract and title. Office Action dated December 14, 2005, p. 7. However, the Examiner's interpretation of this cited reference is incorrect.

The cited portion of *Reeve* is as follows:

> **Small Computer Systems Interface-Data Link Processor**
> A peripheral controller executes data transfer operations between a host computer and a multiple number of separate peripheral terminal units. A specialized buffer memory control system provides dedicated page-segments for each one of the peripheral terminal units to enable the peripheral controller to concurrently manage a multiple number of data transfer cycles in an optimum fashion in order to increase the through-put of the data transfer operations.

As can be seen, this portion of *Reeve* teaches that a specialized buffer memory control system enables a peripheral controller to increase the through-put of the data transfer operations. However, neither the cited portion of *Reeve*, nor any other portion of *Reeve* makes mention of receiving within the storage drive the command to *verify* the condition of the storage drive's media utilizing the SCSI bus, as recited in claim 9. Therefore, *Reeve* does not teach or suggest the features of claim 9, as asserted by the Examiner. In addition, *Reeve* does not elsewhere teach or suggest the claimed features, as asserted by the Examiner.

II.A.3 The Examiner Has Failed to State Proper Motivation to Combine the References

In addition, assuming *arguendo* that *Jeddeloh* does teach the step of receiving a command to verify the condition of the storage drive's media, these two references cannot be combined as suggested by the Examiner. In combining these two references, the Examiner states:

> Therefore it would have been obvious to one of ordinary skill in the art, to utilize a SCSI bus, as taught by Reeve, because SCSI controls information transfer between a host computer system and certain compatible target devices.

This statement is not a proper motivation to combine the references or to further modify the proposed combination to reach the present invention of claims 6 and 9. The Examiner has only presented an advantage to combining the two cited references. An advantage cannot be substituted for a motivation to combine references because an advantage is not necessarily a motivation. Just because it is advantageous to modify or combine references does not mean there exists a motivation to perform the modification or combination.

For example, a first reference may disclose the use of lasers to achieve nuclear fusion. A second reference may disclose that an ultra-high power laser delivers more energy. One of ordinary skill may recognize that an ultra-high power laser would be more useful to achieve nuclear fusion, though one of ordinary skill would be motivated to avoid combining the references because of the extreme expense of ultra-high power lasers. In this example, one of ordinary skill is motivated to avoid implementing the combination, even if he or she recognized the advantage, and so no motivation exists to combine the references. In the case at hand, the Examiner has not provided any reason why one of ordinary skill would recognize the proposed advantage or have a reason to implement it. For this reason, the Examiner's statement fails to provide a proper motivation to combine the references. Accordingly, the Examiner has failed to state a prima facie obviousness rejection.

Further, no teaching, suggestion, or incentive based on the prior art has been pointed out to combine these two references. The "motivation" presented is based only on the Examiner's statement, and is without any teaching, suggestion, or incentive based on the prior art. The Examiner's motivation alone, without any teaching, suggestion, or incentive based on the prior art, is insufficient to combine these two references.

Furthermore, the Examiner's statement is logically insufficient to make the suggested modification or combination because the Examiner is using the feature itself as motivation. The Examiner states that a person of ordinary skill in the art would combine the teachings of *Jeddeloh* and *Reeve* to receive a command to verify the condition of the storage drive's media, the motivation being because SCSI controls information transfer between a host computer system and certain compatible target devices. A feature of the SCSI bus cannot itself be used as the motivation to combine the references. Therefore, the Examiner has failed to state a proper motivation to combine the references.

Also, the Examiner has failed to state a proper motivation because the reference does not teach the features that the Examiner believes are disclosed. As established above, neither *Jeddeloh* nor *Reeve* mention receiving a command to verify the condition of the storage drive's media, as recited in claim 6 and claim 9. Because this teaching is not present in *Jeddeloh* or *Reeve*, and because the Examiner has not shown a motivation to further modify the proposed combination, the Examiner has failed to supply a motivation based on the actual teachings of the references. Hence, the Examiner has failed to state a proper motivation to combine the

references and, accordingly, has failed to state a *prima facie* obviousness rejection against claims 6 and 9.

II.B. Claim 6 and Claim 9 are Non-Obvious in View of *Jeddeloh* and *Reeve*

"It is impermissible within the framework of section 103 to pick and choose from any one reference only so much of it as will support a given position, to the exclusion of other parts necessary to the full appreciation of what such reference fairly suggests to one of ordinary skill in the art." *In re Hedges*, 228 U.S.P.Q. 685, 687 (Fed. Cir. 1986). In viewing the references as a whole, one of ordinary skill would look to the problems addressed by the references in determining whether to combine the references. *Jedddeloh* and *Reeve* address different problems than the present invention.

Jeddeloh relates to a memory module having a volatile memory block, a nonvolatile memory block having an error map, and a remapping table included in the volatile memory block (*Jedddeloh*, claim 1). Figure 1 of *Jeddeloh* shows a block diagram of a computer system in which memory module **12** and hard drive **32** are distinct and separate components of the computer system. *Jeddeloh*, Figure 1. *Jeddeloh* teaches receiving a *write* data request or a *read* data request from a portion of a volatile memory block. *Jeddeloh*: step 64, Fig. 3; Col. 5, Lines 51-56. In contrast, the present invention of claim 6 and claim 9 deals with receiving a command to *verify* the storage driver's media.

Jeddeloh is concerned with using an error map when accessing memory module 12. *Jeddeloh*, claim 1. In *Jeddeloh*, the memory controller determines whether a requested volatile memory portion is one of the defective memory portions. *Jeddeloh*, claim 1. In contrast, in the present inventions of claim 6 and claim 9, the verifying is done by the storage drive.

Furthermore, in *Jeddeloh*, hard drive **32** is described as a *nonvolatile* memory device while memory module **12** contains *volatile* memory block **14**. "The hard drive **32** in effect, is a nonvolatile memory device that stores data and computer instructions that are processed by the computer processor **24** after the data and computer are transferred to the volatile memory block **14** of the memory module **12**." *Jeddeloh* col. 3, lines 28-32.

In summary, *Jeddeloh* relates to receiving a read or write request, the memory controller determines whether a requested volatile memory portion is one of the defective memory portions, and any actions are performed on the memory module component of the computer system. In

contrast, the inventions of claim 6 and claim 9 have to do with receiving a verify command, the verifying is done by the storage drive, and the verifying is done to the storage drive's media. Thus the command received, the component performing the action, and the component on which the action is performed are entirely different in *Jeddeloh* than the inventions of claim 6 and claim 9.

Similarly, *Reeve* relates to using a data link processor and specialized buffer memory control system to manage multiple data transfers to increase the throughput of data transfers. *Reeve*, Abstract. *Reeve* accomplishes an increase in the throughput of data transfers by providing "for the temporary storage of data being transferred, by temporarily holding it in a segmented RAM buffered memory". *Reeve* Column 1, Lines 63-66. Increasing the throughput of data transfers is unrelated to verifying the condition of a storage drive's media.

Reeve is directed to a data link processor which controls data transfers to peripherals such as magnetic disks. *Reeve*, Abstract. In contrast, the inventions of claim 6 and claim 9 have to do with receiving a verify command, and the verifying is done by the storage drive. Thus, the command received and the component performing the action is entirely different in *Reeve* than in the inventions of claim 6 and claim 9.

Therefore, both *Jeddeloh* and *Reeve* address different problems than the inventions of claim 6 and claim 9. Thus, no one of ordinary skill would be motivated to look to either *Jeddeloh* or *Reeve* to verify a condition of a storage drive's media. Similarly, no one of ordinary skill would be motivated to combine either *Jeddeloh* or *Reeve* or to further modify the combination to achieve the features of claim 6 or claim 9. Accordingly, claim 6 and claim 9 are non-obvious in view of the cited references when the references are considered as a whole.

II.C. **Conclusion as to Asserted Obviousness of Claims 6-9, 22-25, and 38-41**

Both claim 6 and claim 9 deal with receiving a command to verify a storage driver's media. However, neither *Jeddeloh* nor *Reeve* make mention of receiving a verify command nor of verifying a shortage driver's media. Because claims 7 and 8 depend from claim 6, the same distinctions between *Jedddeloh*, *Reeve* and the invention of claim 6 can be made for these claims. Consequently, Applicants respectfully urge that the rejection of claims 6-9 has been overcome.

Similarly, claims 22-25 claim data processing systems implementing the methods of claims 6-9. Therefore, the same distinctions between *Reeve* and the inventions of claims 6-9 can

be made for claims 22-25. Consequently, Applicants respectfully urge that the rejection of claims 22-25 has been overcome.

Claims 38-41 claim computer program products implementing the methods of claims 6-9. Therefore, the same distinctions between *Jeddeloh*, *Reeve* and the inventions of claims 1-16 can be made for claims 38-41. Consequently, Applicants respectfully urge that the rejection of claims 38-41 has been overcome. Therefore, the rejection of claims 6-9, 22-25, and 38-41 under 35 U.S.C. § 103(a) has been overcome.

III. 35 U.S.C. § 103, Asserted Obviousness, Claims 10, 26, and 42

The Examiner rejected claims 10, 26, and 42 under 35 U.S.C. § 103(a) as obvious over *Jeddeloh* in view of *Russell* et al., Recovering and Relocating Unreliable Disk Sectors When Encountering Disk Drive Read Errors, U.S. Patent No. 6,332,204, (Sep. 21, 1987) (hereinafter "*Russell*"). This rejection is respectfully traversed.

With regards to claims 10, 26, and 42, the Examiner states:

> Jeddeloh discloses the use of an error table to reassign logical block addresses; but fails to specifically teach determining block addresses that require error recovery procedures. However, Russell discloses determining logical block addresses that require error recovery procedures and reassigning block addresses that require error recovery procedures [abstract; Col. 2, Lines 22-26]. Therefore, it would have been obvious to one of ordinary skill in the art, to recover failing sectors because data within a failing sector could be recovered before the sector becomes completely unrecoverable, as taught by Russell [Col. 2, Lines 26-29].

Office Action dated December 14, 2005, page 7.

Claim 10 is as follows:

> 10. The method according to claim 1, further comprising the steps of:
> determining, by said storage drive, ones of said plurality of logical block addresses that require error recovery procedures; and
> reassigning said ones of said plurality of logical block addresses that require error recovery procedures.

Claim 10 depends from claim 1, and claim 1 is as follows:

> 1. A method in a storage drive for verifying a condition of said storage drive's media, said method comprising the steps of:
> receiving within said storage drive a command to verify said condition of said storage drive's media;
> in response to a receipt of said command, attempting, by said storage drive, to read each one of a plurality of logical block addresses included in said

storage drive; and

verifying said condition of said media by determining, by said storage drive, ones of said plurality of logical block addresses that are not in a readable condition.

The features that the Examiner states as being present in the references are not found or suggested by the references. *Russell* fails to teach the claimed step of receiving a command to *verify* the condition of the storage drive's media. The Examiner asserts otherwise, citing the following portion of *Russell*:

> If the threshold number of attempts was equaled or exceeded, however, the unreliable or failing sector is relocated to a reserved replacement sector, with the recovered data written to the replacement sector. The failing data sector is remapped to the replacement sector, which becomes a fully functional substitute for the failing sector for future reads and writes while preserving the original user data. Data within a failing sector is thus preserved before the sector becomes completely unrecoverable.

Russell, Abstract, lines 22-29.

Russell teaches using a threshold number of attempts to determine when a data sector is failing and should be remapped to a replacement sector. However, neither *Jeddeloh* nor *Russell* mention receiving within the storage drive a command to *verify* the condition of the storage drive's media. Thus, all of the features of claim 1, and hence claim 10, which depends from claim 1, are not present in the cited references. Therefore, the Examiner has failed to state a prima facie obviousness rejection against claim 10.

Further, no teaching, suggestion, or incentive based on the prior art has been pointed out to combine these two references. The "motivation" presented is based only on the Examiner's statement, and is without any teaching, suggestion, or incentive based on the prior art. The Examiner's motivation alone, without any teaching, suggestion, or incentive based on the prior art, is insufficient to combine these two references.

Furthermore, the Examiner's statement is logically insufficient to make the suggested modification or combination because the Examiner is using the feature itself as motivation. The Examiner states that a person of ordinary skill in the art would combine the teachings of *Jeddeloh* and *Russell* to receive a command to verify the condition of the storage drive's media, the motivation being because data within a failing sector could be recovered before the sector becomes completely unrecoverable. A feature of *Russell* cannot itself be used as the motivation

to combine the references, unless one of ordinary skill would have a teaching, suggestion, or motivation to use that feature in combination with the primary reference in the claimed manner. Therefore, the Examiner has failed to state a proper motivation to combine the references.

In addition, the Examiner has failed to state a proper motivation because the reference does not teach the features that the Examiner believes are disclosed. Neither *Jeddeloh* nor *Russell* mention receiving a command to verify the condition of the storage drive's media, as recited in claim 1. Because this teaching is not present in *Jeddeloh* or *Russell*, and because the Examiner has not shown a motivation to further modify the proposed combination, the Examiner has failed to supply a motivation based on the actual teachings of the references. Hence, the Examiner has failed to state a proper motivation to combine the references and, accordingly, has failed to state a *prima facie* obviousness rejection against claim 1.

IV. Conclusion

It is respectfully urged that the subject application is patentable over *Jeddeloh*, *Reeve*, and *Russell* and is now in condition for allowance.

The Examiner is invited to call the undersigned at the below-listed telephone number if in the opinion of the Examiner such a telephone conference would expedite or aid the prosecution and examination of this application.

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Respectfully submitted,

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